

REMARKS

In response to the Office Action mailed August 27, 2003 Applicants respectfully request reconsideration. To further the prosecution of this application, claim amendments and arguments are submitted herewith.

Claims 1-60 were pending in this application. Applicants have amended claims 1, 21, 22, and 42. New claims 61-64 have been added. Therefore, claims 1-64 are pending for examination with claims 1, 21, 22, and 42 being independent claims.

Claim Rejections Under 35 U.S.C. §102

Claims 1-60 stand rejected under 35 U.S.C. §102(b) as being purportedly being anticipated by U.S. Patent No. 5,737,516 to Circello et al. (hereinafter Circello). Applicants respectfully traverse this rejection.

A. Discussion of Circello

Circello teaches a data processing system and method for performing a debug function. Figure 1 illustrates a data processing system, as taught by Circello (col. 2, lines 54-56). The data processing system 5 includes a data processor 3 (col. 4, lines 6-7). Data processor 3 contains a core 9 and a debug module 10 (col. 4, lines 7-10), as well as a system bus controller 8 (col. 4, lines 7-9). The core contains a central processing unit (CPU) 2, a memory management unit 4, and a memory 6 (col. 4, lines 17-19). The CPU 2, memory management unit 4, memory 6, and debug module 10 are connected to one another by K-Bus 25 (col. 4, lines 19-21). The CPU 2 provides debug module 10 with a CPST signal and a Bus Grant signal, as shown in Figure 1 (col. 4, lines 24-26, lines 53-54).

B. Claim 1 Patentably Distinguishes Over Circello

Claim 1, as amended, is directed to a microcomputer comprising at least one processor, a debug circuit, and a system bus coupling the processor and debug circuit. The microcomputer further comprises a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a

plurality of bit values each representing a state of an operation in the processor including at least an operand address.

Circello fails to teach all the limitations of claim 1. For instance, the Office Action asserts that the claimed system bus reads on system bus controller 8 of Circello. Applicants respectfully disagree. System bus controller 8 of Circello is not a system bus, but is rather a system bus controller. The claimed system bus couples the processor and the debug circuit. In light of this fact, and the fact that the Office Action asserts that the claimed communication link reads on "all connections/bus between core 9 and the debug module 10," of Circello (Office Action, page 3), Applicants respectfully contend that Circello fails to teach the claimed system bus **and** communication link. Thus, claim 1 distinguishes over Circello.

Yet, even if one were to construe Circello as teaching the claimed system bus and communication link, Circello still would not teach all the limitations of claim 1. Specifically, the claimed processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor **including at least an operand address**. Applicants respectfully contend that Circello fails to teach this limitation. As mentioned above, in the discussion of Circello, the CPU 2 of Circello provides debug module 10 with a CPST signal and a Bus Grant signal (col. 4, lines 24-26, lines 53-54). There is no teaching of the CPU 2 providing debug module 10 with an operand address. The Office Action refers to column 3, lines 54-65 of Circello, a portion of which reads:

In the following description of the connectivity of the present invention, the term "bus" will be used to refer to a plurality of signals or conductors, which may be used to transfer one or more various types of information, such as data, addresses, control, or status. (col. 3, lines 55-59)

There is no teaching of the claimed operand address in this portion of Circello. Thus, claim 1 distinguishes over Circello for at least the cited limitations. Accordingly, Applicants respectfully request that the rejection of claim 1 under 35 U.S.C. §102(b) be withdrawn.

Claims 2-20, and new claim 61 depend from claim 1, and are allowable for at least the same reasons.

C. Claim 21 Patentably Distinguishes Over Circello

Claim 21, as amended, is directed to a microcomputer implemented on a single integrated circuit. The microcomputer comprises, *inter alia*, at least one processor, a debug circuit, a system bus coupling the processor and debug circuit, and a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of an operand address and an operand value.

As discussed above in connection with claim 1, Circello does not teach processor configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor **including at least one of an operand address and an operand value**. Neither the circuit shown in Figure 1, nor the portions of Circello referred to by the Office Action, specifically column 3, lines 54-65, teach this limitation. Accordingly, Applicants respectfully request that the rejection of claim 21 under 35 U.S.C. §102(b) be withdrawn.

New claim 62 depends from claim 21 and is allowable for at least the same reasons.

D. Claim 22 Patentably Distinguishes Over Circello

Claim 22, as amended, is directed to a microcomputer comprising, at least one processor, a debug circuit, and a system bus coupling the processor and debug circuit. The microcomputer further comprises means for transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address. As discussed previously in connection with claim 1, Circello fails to teach means for transmitting to the debug circuit a plurality of bit values **including at least an operand address**. Thus, Applicants respectfully request that the rejection of claim 22 under 35 U.S.C. §102(b) be withdrawn.

Claims 23-41 and new claim 63 depend from claim 22 and are allowable for at least the same reasons.

E. Claim 42 Patentably Distinguishes Over Circello

Claim 42, as amended, recites a method for transferring information between a processor and a debug circuit over a communication link. The method comprises transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address. The method further comprises transmitting a program counter value indicating the program counter of the processor.

As discussed above in connection with claim 1, Circello does not teach transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor **including at least an operand address**. Accordingly, Applicants respectfully request that the rejection of claim 42 under 35 U.S.C. §102(b) be withdrawn.

Claims 43-60, and new claim 64 depend from claim 42 and are allowable for at least the same reasons.

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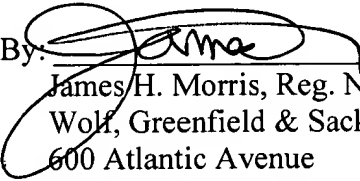
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CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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